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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/520,929	01/11/2005	Yuuko Oono	SON-2787	4819
23353	7590	08/28/2007	EXAMINER	
RADER FISHMAN & GRAUER PLLC			SINGH, HIRDEPAL	
LION BUILDING			ART UNIT	PAPER NUMBER
1233 20TH STREET N.W., SUITE 501			2611	
WASHINGTON, DC 20036			MAIL DATE	DELIVERY MODE
			08/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/520,929	OONO ET AL.
	Examiner Hirdepal Singh	Art Unit 2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 11 January 2005.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-3 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-3 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 11 January 2005 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 1/11/05
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) Notice of Informal Patent Application
- 6) Other: _____

DETAILED ACTION

This action is in response to the preliminary amendment filed on February 07,2006.

Claims 1-3 are pending and have been considered below.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shim et al. (US 6,560,302) in view of Shimizume et al. (US 4,979,192).

Regarding Claim 1:

Shim et al discloses a synchronization signal detection apparatus (figure 3) characterized by comprising:

interpolation means (232 in figure 5) for interpolating a synchronization signal generated according to detection timing of said synchronization signal detected by said synchronization signal detection means as a reproducing synchronization signal when said synchronization signal detection means is unable to detect any synchronization

signal (column 3, lines 52-55; column 4, lines 30-38) within a predetermined detection period;

judgment mean (224, 232 and 234 in figure 5) for performing judgment about whether said synchronization signal continuously detected by said synchronization signal detection means is at normal timing or not under a predetermined condition (214, 216 and 218 in figure 3; column 3, lines 60-67 "the switching circuit's output is in accordance with the defect i.e. whether the defect is detected or not i.e. the sync signal is detected or not") after a start of the interpolation of said synchronization signal by said interpolation means; and

resynchronization means (230 in figure 5) for outputting said synchronization signal detected by said synchronization signal detection means as a reproducing synchronization signal according to a judgment result (column 4, lines 39-48; "the sync signal outputted by 230 in figure 5 is in accordance with the judgment if it is the sync insertion/interpolation signal or sync detection signal") of said judgment means.

Shim et al discloses all of the subject matter as described above except for specifically teaching synchronization signal detection means for inputting a signal formed by a frame in accordance with a predetermined format to detect a synchronization signal to be inserted into said frame.

However, Shimizume et al in same filed of endeavor discloses synchronization signal detection means (34 in figure 3) for inputting a signal formed by a frame in accordance with a predetermined format to detect a synchronization signal to be inserted into said frame (column 3, lines 55-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a synchronization signal detector as taught by Shimizume in Shim system in order to get the information whether frame synchronizing signal is present to generate a window function to insert or interpolate a synchronization signal in case there is lack of frame synchronizing signal, the synchronization signal detector makes the synchronizing signal detection and interpolation stable.

Regarding Claim 2:

Shim et al discloses all of the subject matter as described above and further discloses that judgment means is configured to perform judgment about whether each of said synchronization signal is at normal timing or not;

by measuring an interval of detection timing of said synchronization signal continuously detected (column 4, lines 50-62; "the counter counts the bits during sync detection, comparator compares the count from register to normal sync signal") by said synchronization signal detection means; and

by performing judgment about whether said interval of detection timing coincides with a predetermined interval and a predetermined times or more (column 4, lines 65-67; column 5, lines 1-18) in accordance with an input signal format.

Regarding Claim 3:

Shim et al discloses a synchronization signal detection method characterized by comprising the steps of executing:

an interpolation process for interpolating a synchronization signal generated according to detection timing of the synchronization signal detected by the synchronization signal detection process as a reproducing synchronization signal when no synchronization signal has been able to be detected within a predetermined detection period (column 3, lines 52-55; column 4, lines 30-38) by the synchronization signal detection process;

a judgment process for performing judgment about whether the synchronization signal continuously detected by the synchronization signal detection process is at normal timing or not under a predetermined condition (column 3, lines 60-67 “the switching circuit’s output is in accordance with the defect i.e. whether the defect is detected or not i.e. the sync signal is detected or not”) after a start of the interpolation of the synchronization signal by the interpolation process; and

resynchronization process for outputting the synchronization signal detected by the synchronization signal detection process as the reproducing synchronization signal (column 4, lines 39-48) according to a judgment result of the judgment process.

Shim et al discloses all of the subject matter as described above except for specifically teaching synchronization signal detection means for inputting a signal formed by a frame in accordance with a predetermined format to detect a synchronization signal to be inserted into said frame.

However, Shimizume et al in same filed of endeavor discloses synchronization signal detection means (34 in figure 3) for inputting a signal formed by a frame in

accordance with a predetermined format to detect a synchronization signal to be inserted into said frame (column 3, lines 55-60).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to use a synchronization signal detector in order to get the information whether frame synchronizing signal is present to generate a window function to insert or interpolate a synchronization signal in case there is lack of frame synchronizing signal, the synchronization signal detector makes the synchronizing signal detection and interpolation stable.

Conclusion

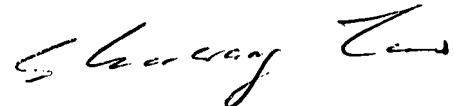
1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
 - a. Karino (US 5,677,935) discloses a synchronization detection circuit and method.
 - b. Kobayashi et al (US 6,963,529) discloses a method and apparatus for reproducing data by using synchronizing detection and protection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hirdepal Singh whose telephone number is 571-270-1688. The examiner can normally be reached on Mon-Fri (Alternate Friday Off)8:00AM-5:00PMEST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HS
August 22, 2007



SHUWANG LIU
SUPERVISORY PATENT EXAMINER